Access DB# 70850

SEARCH REQUEST FORM

Scientific and Technical Information Center

Requester's Full Name: P. Laufer Examiner#: 73139 Date: 7/15/02

Art Unit: 2100 Phone Number: 306 4160 Serial Number: 10/006,939

Mail Box and Bldg/Room Location: _____ Results Format Preferred (circle): Paper Disk E-mail

If more than one search is submitted, please prioritize searches in order of need.

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Please provide a detailed statement of the search topic, and describe as specifically as possible the subject matter to be searched. Include the elected species or structures, keywords, synonyms, acronyms, and registry numbers, and combine with the concept or utility of the invention. Define any terms that may have a special meaning. Give examples or relevant citations, authors, etc., if known. Please attach a copy of the cover sheet, pertinent claims, and abstract.

Title of Invention: _____

Inventors (please provide full names): _____

_____

Earliest Priority Filing Date: _____

**For Sequence Searches Only* Please include all pertinent information (parent, child, divisional, or issued patent numbers) along with the appropriate serial number.*

Litigation

5,996,036

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STAFF USE ONLY

Searcher: S Green

Searcher Phone: 6-4767

Searcher Location: 4B40

Date Searcher Picked Up: 7-15-02

Date Completed: 7-15-02

Searcher Prep & Review Time: 2

Clerical Prep Time: _____

Online Time: 8

Type of search

NA Sequence (#) _____

AA Sequence (#) _____

Structure (#) _____

Bibliographic _____

Litigation ✓

Full Text _____

Patent Family _____

Other _____

Vendors and cost where applicable

STN _____

Dialog _____

Questel/Orbit 23.82

Dr. Link _____

Lexis/Nexis _____

Sequence System _____

WWW/Internet _____

Other (specify) _____

1 of 1 DOCUMENT

UNITED STATES PATENT AND TRADEMARK OFFICE GRANTED PATENT

5996036

November 30, 1999

Bus transaction reordering in a computer system having unordered slaves

REISSUE: November 30, 2001 - Reissue Application filed Ex. Gp.: 2181; Re. S.N. 10/006,939June 18, 2002

INVENTOR: Kelly, James D., Aptos, CA

APPL-NO: 08779632

FILED-DATE: January 7, 1997

GRANTED-DATE: November 30, 1999

ASSIGNEE-AT-ISSUE: Apple Computers, Inc., Cupertino, CA

ASSIGNEE-AFTER-ISSUE: April 2, 1999 - ASSIGNMENT OF ASSIGNOR'S INTEREST (SEE DOCUMENT FOR DETAILS)., APPLE COMPUTER, INC. ONE INFINITE LOOP CUPERTINO, CALIFORNIA 95014,, Reel and Frame Number: 009859/0365

LEGAL-REP: Burns, Doane, Swecker & Mathis, L.L.P.

US-MAIN-CL: 710#110

IPC-MAIN-CL: G 06F009#46

IPC ADDL CL: G 06F013#36, G 11C007#0

SEARCH-FLD: 710##110 , 710##107 , 710##263 , 710##41 , 710##52 , 711##151 , 709##100-102 , 709##208

PRIM-EXMR: Ray, Gopal C.

CORE TERMS: bus, bridge, master, slave, queue, deadlock, arbiter, memory, bit, tenure ...

ENGLISH-ABST:
A mechanism is provided for reordering bus transactions to increase bus utilization in a computer system in which a split- transaction bus is bridged to a single-envelope bus. In one embodiment, both masters and slaves are ordered, simplifying implementation. In another embodiment, the system is more loosely coupled with only masters being ordered. Greater bus utilization is thereby achieved. To avoid deadlock, transactions begun on the split-transaction bus are monitored. When a combination of transactions would, if a predetermined further transaction were to begin, result in deadlock, this condition is detected. In the more tightly coupled system, the predetermined further transaction, if it is requested, is refused, thereby avoiding deadlock. In the more loosely- coupled system, the flexibility afforded by unordered slaves is taken advantage of to, in the typical case, reorder the transactions and avoid deadlock without killing any transaction. Where a data dependency exists that would prevent such reordering, the further transactions is killed as in the more tightly-coupled embodiment. Data dependencies are detected in accordance with address-coincidence signals generated by slave devices on a cache-line basis. In accordance with a further optimization, at least one slave device (e.g., DRAM) generates page-coincidence bits. When two transactions to the slave device are to the same address page, the transactions are reordered if necessary to ensure that they are executed one after another without any intervening transaction. Latency of the slave is thereby reduced.

No Documents Found

No documents were found for your search (**5996036 or 5,996,036**). Please edit your search and try again. You may want to try one or more of the following:

- Check for spelling errors.
- Remove some search terms.
- Use more common search terms.
- If applicable, look for all dates.

Edit Search

LEXIS-NEXIS
Library: PATENT
File: CASES

No Documents Found

No documents were found for your search (**5996036 or 5,996,036**). Please edit your search and try again. You may want to try one or more of the following:

- Check for spelling errors.
- Remove some search terms.
- Use more common search terms.
- If applicable, look for all dates.

Edit Search

LEXIS-NEXIS
Library: PATENT
File: JNLS

fam us5996036/pn

1 Patent Groups
** SS 2: Results 1

Search statement 3

?famstate nonstop

1/1 INPADOC - (C) INPADOC
PN - US 5996036 A 19991130 [US5996036]
TI - BUS TRANSACTION REORDERING IN A COMPUTER SYSTEM HAVING UNORDERED SLAVES
IN - KELLY JAMES D [US]
PA - APPLE COMPUTERS INC [US]
AP - US 779632/97-A 19970107 [1997US-0779632]
PR - US 779632/97-A 19970107 [1997US-0779632]
IC - G06F-009/46; G06F-013/36; G11C-007/00

1/1 LEGALI - (C) LEGSTAT
PN - US 5996036 [US5996036]
AP - US 779632/97 19970107 [1997US-0779632]
DT - US-P
ACTE- 19970107 US/AE-A
APPLICATION DATA (PATENT)
{US 779632/97 19970107 [1997US-0779632]}
- 19991130 US/A
PATENT
- 20020618 US/RF
REISSUE APPLICATION FILED
20011130
UP - 2002-26

Search statement 3

us5996036/pn

** SS 2: Results 1

Search statement 3

?prt full nonstop legalall

1/1 PLUSPAT - (C) QUESTEL-ORBIT
PN - US5996036 A 19991130 [US5996036]
TI - (A) Bus transaction reordering in a computer system having unordered slaves
PA - (A) APPLE COMPUTERS INC (US)
IN - (A) KELLY JAMES D (US)
AP - US77963297 19970107 [1997US-0779632]
PR - US77963297 19970107 [1997US-0779632]
IC - (A) G06F-009/46 G06F-013/36 G11C-007/00
EC - G06F-013/40D1R
PCL - ORIGINAL (O) : 710110000; CROSS-REFERENCE (X) : 709208000 710107000
DT - Basic
CT - US4181974; US4473880; US4965716; US5006982; US5191649; US5257356; US5287477; US5327538; US5345562; US5375215; US5473762; US5592631; US5682512; US5822772
STG - (A) United States patent
AB - A mechanism is provided for reordering bus transactions to increase bus utilization in a computer system in which a split-transaction bus is bridged to a single-envelope bus. In one embodiment, both masters and slaves are ordered, simplifying implementation. In another embodiment, the system is more loosely coupled with only masters being ordered. Greater bus utilization is thereby achieved. To avoid deadlock, transactions begun on the split-transaction bus are monitored. When a combination of transactions would, if a predetermined further transaction were to begin, result in deadlock, this condition is detected. In the more tightly coupled system, the predetermined further transaction, if it is requested, is refused, thereby avoiding deadlock. In the more loosely-coupled system, the flexibility afforded by unordered slaves is taken advantage of to, in the typical case, reorder the transactions and avoid deadlock without killing any transaction. Where a data dependency exists that would prevent such reordering, the further transactions is killed as in the more tightly-coupled embodiment. Data dependencies are detected in accordance with address-coincidence signals generated by slave devices on a cache-line basis. In accordance with a further optimization, at least one slave device (e.g., DRAM) generates page-coincidence bits. When two transactions to the slave device are to the same address page, the transactions are reordered if necessary to ensure that they are executed one after another without any intervening transaction. Latency of the slave is thereby reduced.

1/1 LGST - (C) LEGSTAT
PN - US 5996036 [US5996036]
AP - US 779632/97 19970107 [1997US-0779632]
DT - US-P
ACT - 19970107 US/AE-A
APPLICATION DATA (PATENT)
{US 779632/97 19970107 [1997US-0779632]}
- 19991130 US/A
PATENT
- 20020618 US/RF
REISSUE APPLICATION FILED
20011130
UP - 2002-26

1/1 CRXX - (C) CLAIMS/RRX
PN - 5,996,036 A 19991130 [US5996036]
PA - Apple Computer Inc
ACT - 20011130 REISSUE REQUESTED
ISSUE DATE OF O.G.: 20020618
REISSUE REQUEST NUMBER: 10/006939
EXAMINATION GROUP RESPONSIBLE FOR REISSUEPROCESS: 2181

Reissue Patent Number:

1/1 PAST - (C) Thomson Derwent
AN - 200225-001697
PN - 5996036 A [US5996036]
OG - 2002-06-18
ACT - REISSUE APPLICATION FILED